**ECE 3457**

**Lab 5: CMOS Transmission Gates**

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**Goal:**

Study CMOS transmission gates.

**Task A:**

Measure the transmission characteristics of CMOS transmission gate. Measure the outputs for inputs ranging from 0 to 5 volts in 1-volt steps.

**Task B:**

Design and measure the response of an XOR and an XNOR gate. Use VDD = 5[V]. Construct a logic table for each gate by applying combinations of 0 and 5[V] inputs and recording the output voltages.

**Task C:**

Simulate the circuits using PSPICE or MultiSim or your favourite simulator.

**Theory:**

From Lab 1: (used to find simulation characteristics for transistors)

The CD4007 enhancement nMOS and pMOS transistors have gate, drain, and source pins. The transistor has the equations

for when the transistor is operating in the triode region (VGS > VT and VDS ≤ VGS – VT) and

for when the transistor is operating in the saturation region (VGS > VT and VDS > VGS – VT). As the transistor enters the saturation region, the ID curve will begin to plateau. This is because the equation for current through the drain and source pins is not dependent on VDS when the transistor is operating in the saturation region. By obtaining the nMOS and pMOS transistors’ iv curves for different VGS values, it becomes possible to derive the value of K where

We can calculate the value of K and VT by plotting the square root of IDS against VGS according to the linear equation

Where the square root of K is the slope and VT is the x-intercept.

Lab 4: (Task B & C)

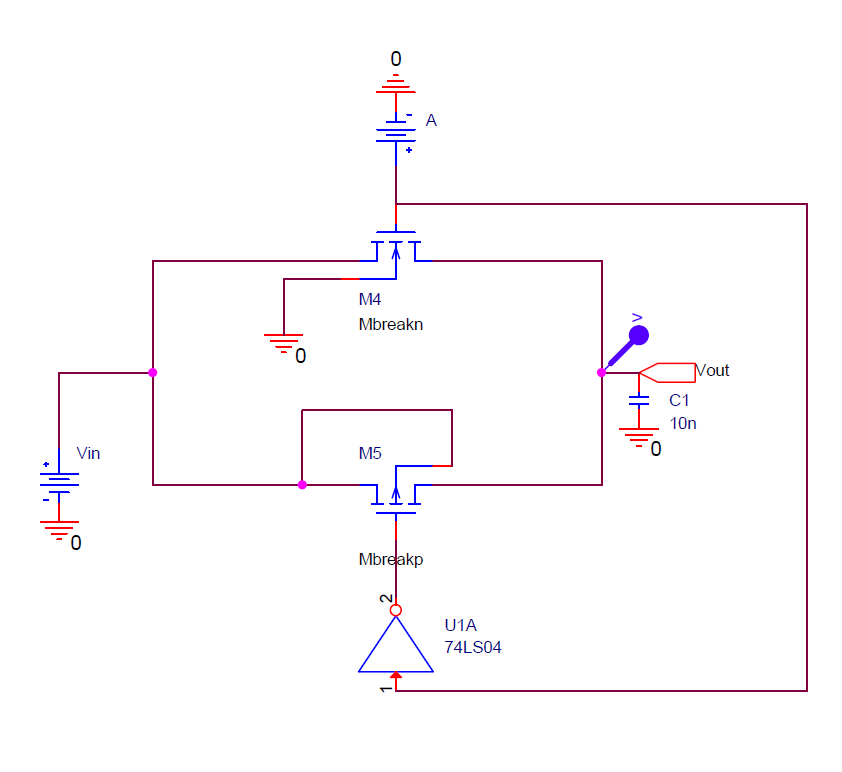
A transistor has 3 states: cut-off region, triode region, and saturation region. The transistor acts as an open circuit in the cut-off region, as such no current will flow. In the triode region, the current varies so the voltage across the transistor will also vary. When the transistor is operating in saturation mode, its current should no longer be changing dramatically so it acts like a small resistor, resulting in a small voltage reading across the transistor. As the transistor acts like an open circuit in the cut off region, it can be used like a logic switch by varying the gate voltage. A CMOS gate will allow current flow when the gate voltage passes the required threshold. By stacking CMOS transmission gates, it is possible to realise different logical functions.

**Simulation & Experiment:**

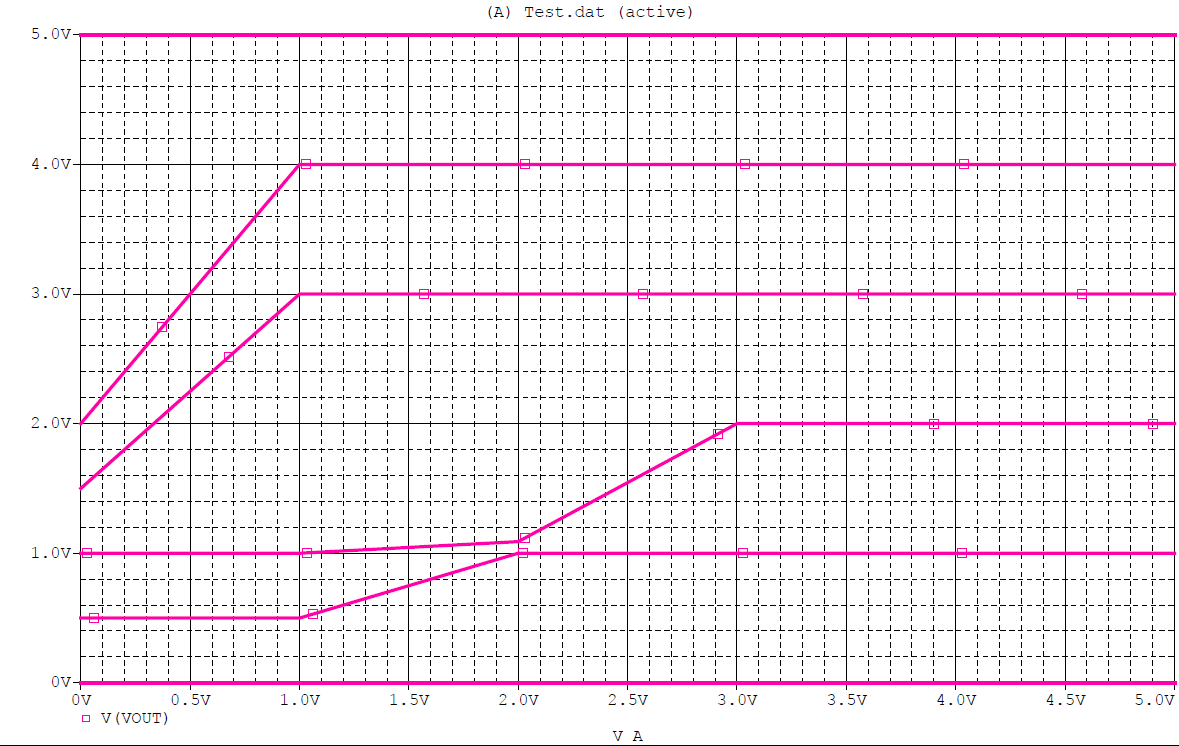
For all tasks following, simulation values were found in Lab 1. The values for the nMOS are Kn is 685.6[μA/V2], and VT is 0.91[V]. The values for the pMOS are Kp is 635.2[μA/V2], and VT is 1.32 [V].

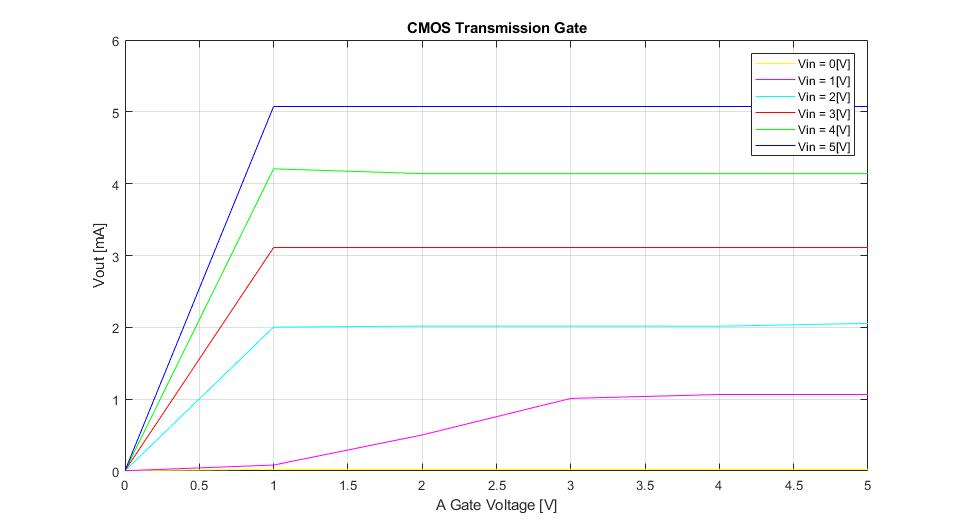
**Task A: CMOS Transmission Gate:**

The circuit was designed such that there would be two inputs, a gate voltage (A) and an input voltage (Vin). The voltage was measured at Vout and data recorded. The below circuit is the CMOS transmission gate which was built.

 *Figure 1: CMOS Transmission Gate*

The inputs to gate A and input voltage Vin are varied between 0[V] and 5[V] in 1[V] increments. The following graphs were retrieved from simulation and experiment.

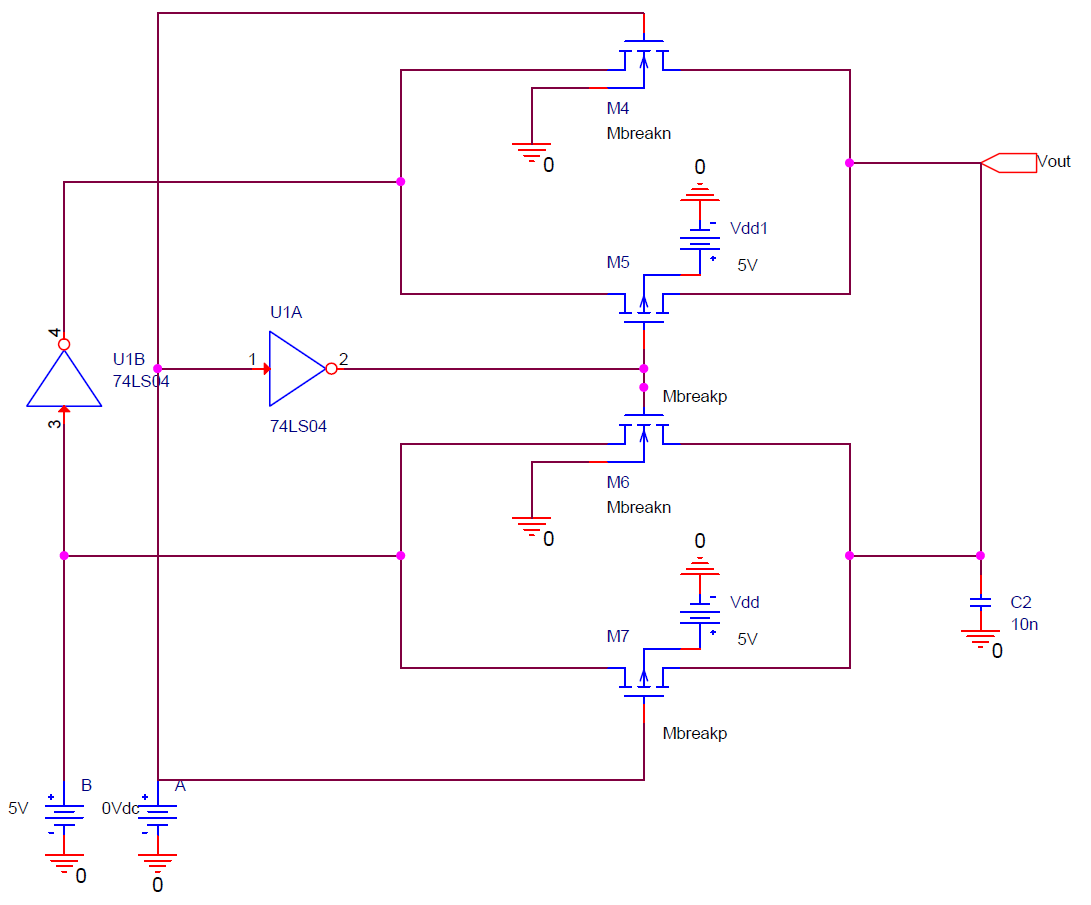
 *Figure 2: Simulated CMOS Transmission Gate Output*

*  
Figure 3: Measured CMOS Transmission Gate Output*

**Task B/C**

**XOR Gate:**

The circuit was designed such that there would be two inputs, A and B, which would be used to simulate a logic function and the output would be measured at Vout. The below circuit realises the logic equation Vout = A⊕B commonly known as an XOR gate.

*Figure 4: XOR Gate Realised Using CMOS Transmission Gates*

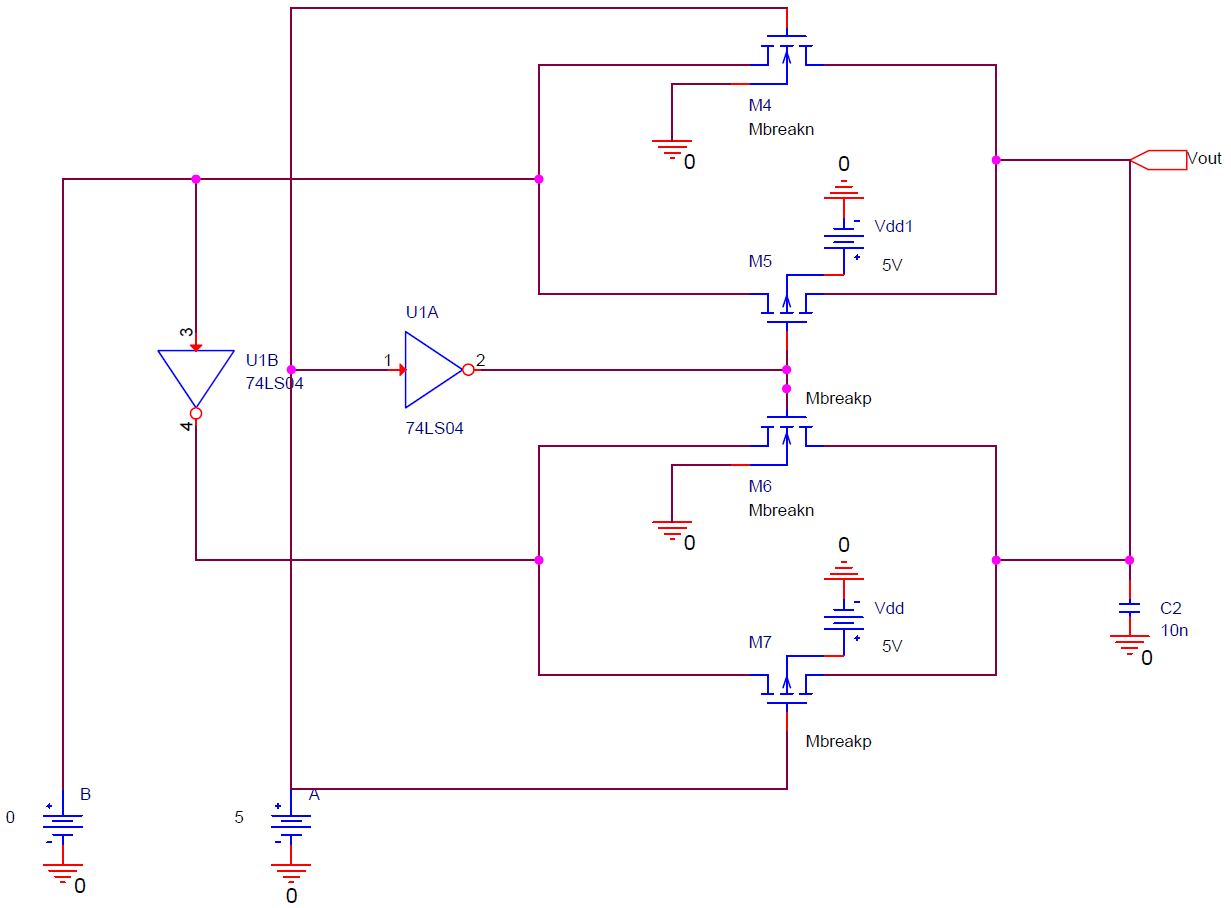
The following data was retrieved from simulations and experiments. Logic level 0 implies an input voltage of 0[V] and logic level 1 implies an input voltage of 5[V].

*Table 1: Output for XOR Gate*

|  |  |  |  |
| --- | --- | --- | --- |
| A [Logic Level] | B [Logic Level] | Vout Simulated [V] | Vout Experiment [V] |
| 0 | 0 | 1.987[nV] | 0.138[mV] |
| 0 | 1 | 4.9932 | 5.0124 |
| 1 | 0 | 3.4493 | 5.0081 |
| 1 | 1 | 0.1015 | 0.214[mV] |

**XNOR Gate:**

The circuit was designed such that there would be two inputs, A and B, which would be used to simulate a logic function and the output would be measured at Vout. The below circuit realises the logic equation Vout = ͞A ͞B+AB commonly known as a XNOR gate.

*Figure 5: XNOR Gate Realised Using CMOS Transmission Gates*

The following data was retrieved from simulations and experiments. Logic level 0 implies an input voltage of 0[V] and logic level 1 implies an input voltage of 5[V].

*Table 2: Output for XNOR Gate*

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | Vout Simulated [V] | Vout Experiment [V] |
| 0 | 0 | 3.4493 | 4.3390 |
| 0 | 1 | 0.1122 | 0.184[mV] |
| 1 | 0 | 3.573[nV] | 0.168[mV] |
| 1 | 1 | 5.0000 | 4.9863 |

**Analysis:**

Simulation Results contrasted with experimental results for Task A, however, I believe in this case the experimental data is more accurate than the simulated data. I do not believe the simulated circuit was correctly designed and therefore results are not accurate. I believe the issue arises from the differing substrate connections for the experiment and simulation. The output for the experimental results matches those of the simulated results for high gate voltages, however, results drastically differ for low gate voltages. This may have affected simulations for Tasks B and C, but the data suggests that the designed circuit functions more similarly to real life expectations when operating at the logic levels 0: 0[V] and 1: 5[V] as the discrepancies were more prominent around 1[V] and 2[V] input voltages. As we are not testing these gate voltages for Tasks B and C, the simulations appear comparable to experimental data. The XOR gate from Task B meets expectations except for the case where A was high, and B was low. For this scenario, the simulated output voltage is slightly lower than the experimental voltage, however, can still be considered as outputting a logic high state thus realising the intended XOR gate. For the XNOR gate, experimental data is meets expectations except for the case where A was low, and B was low. In this case, the experimental data was slightly higher than the simulated data. In both cases the output is registered as logic level high, so the configured circuit realises the XNOR gate configuration.

**Experimental Data for Figure 2:**

Logic 0 = 0[V]

Logic 1 = 5[V]

|  |  |  |
| --- | --- | --- |
| Step A |  |  |
| Vin = 0 | A [V] | Vout [V] |
|  | 0 | 0.00516 |
|  | 1 | 0.0242 |
|  | 2 | 0.02492 |
|  | 3 | 0.02498 |
|  | 4 | 0.02503 |
|  | 5 | 0.02509 |
|  |  |  |
| Vin = 1 | A [V] | Vout [V] |
|  | 0 | 0.00374 |
|  | 1 | 0.0828 |
|  | 2 | 0.5019 |
|  | 3 | 1.0106 |
|  | 4 | 1.0649 |
|  | 5 | 1.06499 |
|  |  |  |
| Vin = 2 | A [V] | Vout [V] |
|  | 0 | 0.00394 |
|  | 1 | 2.003 |
|  | 2 | 2.0168 |
|  | 3 | 2.0163 |
|  | 4 | 2.0158 |
|  | 5 | 2.0554 |
|  |  |  |
| Vin = 3 | A [V] | Vout [V] |
|  | 0 | 0.00483 |
|  | 1 | 3.1107 |
|  | 2 | 3.1106 |
|  | 3 | 3.1105 |
|  | 4 | 3.1105 |
|  | 5 | 3.1105 |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
| Vin = 4 | A [V] | Vout [V] |
|  | 0 | 0.00401 |
|  | 1 | 4.2062 |
|  | 2 | 4.1406 |
|  | 3 | 4.1405 |
|  | 4 | 4.1404 |
|  | 5 | 4.1405 |
|  |  |  |
| Vin = 5 | A [V] | Vout [V] |
|  | 0 | 0.00531 |
|  | 1 | 5.0743 |
|  | 2 | 5.074 |
|  | 3 | 5.074 |
|  | 4 | 5.0739 |
|  | 5 | 5.0738 |